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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,212	05/18/2001	Kozo Nakamura	82821	6761

24628 7590 01/24/2005

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EXAMINER
SONG, MATTHEW J

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,212	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuya et al (JP 6-97179), an English Abstract and Computer translation (CT) have been provided.

Furuya et al discloses a heat-treating method of silicon crystal wafer produced by the Czochralski method (CT [0008]), which is inherently single crystal because the Czochralski process is used to produce single crystalline rods. Furuya et al discloses a low temperature heat treatment with an initiation temperature of 350-450°C (CT [0005]), this reads on applicants' maintaining a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment at less than 500°C. Furuya et al also discloses the low

temperature heat treatment is performed at 650-950°C (CT [0002]), this reads on applicants' temperature in a range of 700-900°C. Furuya et al also discloses the ramping rate during the low temperature heat treatment step is 0.5-2.0°C/min (CT [0009], [0013] and '179 [0009], [0013]). Furuya et al discloses a silicon wafer having a defect free layer (CT [0002]), this reads on applicants' perfect crystal.

Furuya et al discloses ranges of the initial temperature, the heat treatment temperature and the ramping rate. The ranges are not the ranges claimed by applicants, however the ranges overlap the instantly claimed ranges. Overlapping ranges are held to be obvious (MPEP 2144.05).

Referring to claims 10-11, Furuya et al discloses the low temperature treatment is preformed to from a DZ layer on a silicon wafer. Furuya et al does not teach the heat treatment is performed so as to make uniform the distribution of oxide precipitate density of the silicon wafer after heat treatment. This limitation is viewed as an intended use limitation. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. Furthermore, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. It is also noted that uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment would be inherent to Furuya et al because Furuya et al teaches a

similar heat treatment with an ultimate temperature set in a range of 500-900°C at a similar ramping rate of 0.5 °C/min as applicant.

Referring to claims 12-13, Furuya et al teaches the heat treatment was performed on silicon wafer having an oxygen density of $9x10^{17}$ cm^{-3} (CT [0008] and '179 [0008]).

3. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bischoff et al (US 4,437,922).

Bischoff et al teaches a heat treatment method of Czochralski silicon wafers for tailoring oxygen precipitation particle density and distribution (col 1, ln 1-15), this reads on applicants' single crystal wafer because wafers produced using the Czochralski method are inherently single crystalline. Bischoff et al teaches heating from 450°C to 800°C at a rate of 0.84°C/min, this reads on applicants' temperature of less than 500°C. Bischoff et al also teaches annealing at a low temperature of 400-500°C and heating to 750°-1000°C at a rate of less than 2°C/minute or less, specifically a rate of 0.84°C/min (col 4, ln 20-45 and claims 1-3). Overlapping ranges are held to be obvious (MPEP 2144.05).

4. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuya et al (JP 6-97179), an English Abstract and Computer translation (CT) have been provided, or Bischoff et al (US 4,437,922) in view of Iida et al (US 5,968,264) or Adachi et al (US 5,931,662).

Furuya et al or Bischoff et al discloses all of the limitations of claims 9-11, as discussed previously, except the wafer is single crystalline, which the Examiner maintains is inherent. However, if evidence is provided showing that the feature is not inherent, then the claim would

still be unpatentable because the invention would have been obvious in view of Iida et al's teachings.

In a method of forming a single crystal wafer, Iida et al teaches a method of forming a single crystal wafer with very few crystal defects, this reads on applicant's perfect crystal, and when this wafer undergoes an oxygen precipitation heat treatment and is observed by means of X rays, uniform precipitation contrast is observed over the surface thereof and a small number of striation rings is observed (col 13, ln50 to col 14, ln 15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Furuya et al or Bischoff et al with Iida et al's single crystalline silicon wafer to form a uniform precipitation and gettering layer.

In a method of heat treating silicon wafers, Adachi et al teaches heat treating silicon single crystal wafers and annealing is performed to form a defect free (DZ) region (col 10, ln 1-67), this reads on applicants' perfect crystal. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Furuya et al or Bischoff et al with Adachi et al's silicon single crystal wafer because silicon single crystal wafers are conventionally used to in the production of DZ layers.

Response to Arguments

5. Applicant's arguments filed 11/1/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that Furuya has the purpose of controlling the DZ layer, while Applicants are trying to manufacture high quality silicon wafers, the fact that

applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Furuya discloses a heat treatment process, as claimed by applicants; therefore the advantages claimed by Applicants would have naturally flowed from the suggestion of the prior art.

Applicants' argument that the three step process taught by Furuya is different from the claimed process with an initiation temperature up to 500°C is noted but is not found persuasive. Applicants allege that the heat treatment performed at 1150°C, which is different from the first step of a heat treatment up to 500°C. Furuya teaches a ramping heat treatment with an initiation temperature of 350-450°C and a low temperature heat treatment is performed at 650-950°C (CT [0002] and Abstract). The Examiner admits that Furuya teaches heat treating the wafer at 1150°C prior to the ramping treatment, however claims 9-11 utilize "comprising" language; therefore are open to other processing steps. Furuya teaches the claimed first and second steps of the heat treatment; therefore meets the claimed limitation. It is also noted that the omission of an element and its function is held to be obvious if its function is not desired (MPEP 2144.04).

Applicants' argument that the three step process taught by Bischoff is different from the claimed process with an initiation temperature up to 500°C is noted but is not found persuasive. Applicants allege that the heat treatment performed at 1100°C, which is different from the first step of a heat treatment up to 500°C. Bischoff teaches a ramping heat treatment with an initiation temperature of 450°C and a temperature heat treatment is performed at 750-1000°C (Claims 1-4). The Examiner admits that Bischoff teaches heat treating the wafer at 1100°C prior to the ramping treatment, however claims 9-11 utilize "comprising" language; therefore are open to

other processing steps. Furuya teaches the claimed first and second steps of the heat treatment; therefore meets the claimed limitation. It is also noted that the omission of an element and its function is held to be obvious if its function is not desired (MPEP 2144.04).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **only** the second stage heat treatment is performed (pg 6)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Von Ammon et al ("The dependence of bulk defects on the axial temperature gradient of silicon crystal during Czochralski growth") teaches the critical pulling rate varies with the crystal diameter and the type of heat shield (abstract).

Bischoff et al (US 4,437,922) teaches heating a silicon wafer from 450°C to an ultimate temperature of 800°C at a rate 0.84°/min (Fig 2 and claim 8).

Morioka et al (US 4,783,235) teaches to reduce the temperature gradient, the pulling speed should be small in a LEC process for forming single crystals (Abstract and col 10, ln 1-5).

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS
January 14, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER